

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method for processing conditional jump instructions in a processor with pipeline computer architecture, the method comprising:
 - (a) loading and decoding a processor instruction, the processor instruction containing an instruction opcode, register addresses, a relative jump distance, a precondition, which comprises at least one precondition bit that specifies under which conditions the instruction is actually to be executed, and a post-condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked, wherein the post-condition comprises ~~a plurality of post-condition bits~~ at least one post-condition bit that are is checked in the processor;
 - (b) checking the precondition, and ~~execution of~~ executing the decoded processor instruction if the precondition is fulfilled;
 - (c) in the case of a fulfilled precondition, checking the post-condition, and carrying out ~~no-jump~~ no jump if the post-condition is not fulfilled, and checking the corresponding flag bits, if the post-condition is fulfilled; and
 - (d) jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set.

2. (Canceled)

3. (Currently Amended) An apparatus for processing conditional jump instructions in a processor with pipeline computer architecture, the apparatus comprising:

(a) an instruction decoder operable to decode a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition comprising at least one precondition bit configured to specify under which conditions the instruction is actually executed, and a post-condition configured to specify a conditional jump is processed and the corresponding flag bits of an arithmetic-logic unit are to be checked, wherein the post-condition comprises a plurality of post-condition bits at least one post-condition bit that are is checked in the processor, and the precondition comprises at least one precondition bit that is checked in the processor; and

(b) wherein the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled, and, if the post-condition is fulfilled, checking to check corresponding flag bits, if positive, driving and to drive a program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction.